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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,640	03/18/2004	Jung-hee Chung	5649-1188	5341

20792 7590 08/09/2005

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EXAMINER	
TRAN, LONG K	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/803,640	CHUNG ET AL.
	Examiner	Art Unit
	Long K. Tran	2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7 - 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7 - 20* is/are rejected.

7)☒ Claim(s) *7, 8 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/18/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of **Group II**, claims **7 – 20** in the reply filed on June 24, 2005 is acknowledged.

Claims 1 – 6 have been cancelled.

Claims 7 – 20 are presented for examination.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed on March 18, 2004.

Information Disclosure Statement

3. This office acknowledges of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on March 18, 2004.

The references cited on the PTO -1449 form have been considered.

Claim Objections

4. Claim **7** is objected to because of the following informalities:

Line 5, change "on" to --between-- (note: figure 4C clearly illustrates the barrier layer 130 located between dielectric layer 120 and the upper electrode 150. See specification page 5, lines 8 – 9 and page 6, lines 11 – 15).

For examination purposes, the barrier layer in considered being formed between the dielectric layer and the upper electrode.

Line 5, change "the upper" to --an upper--;

Line 7, change "an upper" to --the upper--.

5. Claim **8** is objected to because of the following informalities:

Line 5, change "an upper" to --the upper--;

6. Claim **13** is objected to because of the following informalities Appropriate correction is required.

Line 7, change "a titanium" to --the titanium--.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claim **7** is rejected under 35 U.S.C. 102(b) as being anticipated by Kwon et al. (US Patent No. 5,195,018).

Regarding claim **7**, Kwon discloses a method of forming an integrated circuit device (column 1, lines 7 – 16) comprising:

forming a lower electrode 2 (figure 1A, column 2, lines 60 and 61) of a capacitor C on an integrated circuit substrate 1 (figure 1; column 1, lines 14 – 17 and column 2, lines 53 – 56);

forming a dielectric layer 3 (figure 1B) on the lower electrode 2, the dielectric layer including tantalum oxide (column 2, lines 62 – 67);

forming a barrier layer 4 (figure 1D) between the dielectric layer 3 and an upper electrode 5 (figure 1F), the barrier layer including a titanium oxide layer (column 2, lines 68, 69 and column 3, lines 5 and 6. Note: Kwon does not explicitly show layer 4 is a

barrier layer. However, since layer 4 is made of titanium oxide and is between upper electrode 5and the tantalum oxide layer 3 identical to the instant claim 7, therefore, it is fair to say that layer 4 is a barrier layer); and

forming the upper electrode 5 (figure 1F, column 3, lines 40 – 46) on the dielectric layer 3.

Regarding claim **11**, Kwon discloses the dielectric layer 3 having thickness of from approximately 5 Å to approximately 200 Å (column 2, lines 65 – 67).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claim **9** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon et al. (US Patent No. 5,195,018) in view of Chao et al. (US Patent Application Publication No. 2004/0077142).

Regarding claim **9**, Kwon discloses the claimed invention of claim 7 and forming the dielectric layer comprises forming a tantalum oxide layer 3 over the lower electrode 2 by low pressure chemical vapor deposition, LPCVD, (column 2, lines 62 – 65).

Kwon does not explicitly show forming tantalum oxide layer by CVD.

However, CVD is a traditional method and is a known method in semiconductor art for forming (depositing) dielectric layer of a capacitor as shown by Chao ([0051]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ a traditional well known method shown by Chao to form a tantalum oxide layer of Kwon, since it has been held to be within the general skill of a worker in the art to select a known method on the basis of its suitability for a specific application.

11. Claim **10** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon et al. (US Patent No. 5,195,018) in view of Ahn et al. (US Patent Application Publication No. 2004/0175882).

Regarding claim **10**, Kwon discloses the claimed invention of claim 7 except for forming the dielectric layer 3comprise forming a hafnium oxide layer on the lower electrode by atomic layer deposition (ALD).

However, Ahn shows a method for forming a capacitor that includes forming a dielectric layer containing hafnium oxide on the first conductive layer by ALD ([0096])

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the dielectric layer comprise forming a hafnium oxide layer on the lower electrode by ALD as shown by Ahn to replace the tantalum oxide of Kwon, in order to have minimal reactions with a silicon substrate or other structures (abstract) and to control layer thickness in a straightforward manner by controlling the number of growth cycles by ALD method ([0038]).

12. Claims **15** and **16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon et al. (US Patent No. 5,195,018) in view of Iwasaki et al. (US Patent Application Publication No. 2004/0155276).

Regarding claim **15**, Kwon discloses the claimed invention of claim 7 except for forming the lower electrode 2 of at least one of a doped polysilicon layer, a noble metal layer, and a noble metal oxide layer.

However Iwasaki shows a lower electrode 15 (figure 1; [0071] and [0095]) is formed of ruthenium oxide or iridium oxide (noble metal oxide).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to replace the tungsten lower electrode of Kwon with the noble metal upper electrode of Iwasaki, in order to obtain a means for suppressing diffusion of oxygen to a capacitor electrode ([0071]).

Regarding claim **16**, Kwon discloses the claimed invention of claim 7 except for forming the upper electrode 5 of at least one of Ru, Pt, Ir, Ru oxide, pt oxide and Ir oxide.

However Iwasaki shows an upper electrode 17 (figure 1; [0071] and [0095]) is formed of ruthenium oxide or iridium oxide.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide the tungsten upper electrode of Kwon with the ruthenium oxide or iridium oxide upper electrode of Iwasaki, in order to obtain a means for suppressing diffusion of oxygen to a capacitor electrode ([0071]).

13. Claim **8** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon et al. (US Patent No. 5,195,018) in view of Lin et al. (US Patent Application Publication No. 2004/0262663).

Regarding claim **8**, Kwon discloses forming the barrier layer and the upper electrode further comprising:

forming the titanium oxide layer 4 on the dielectric layer 3 (column 2, lines 68, 69 and column 3, lines 5 and 6);

thermal treatment the dielectric layer 3 and the titanium oxide layer 4 (column 3, lines 47 – 50);

forming the upper electrode 5 on the titanium oxide layer 4 (column 3, lines 40 – 42).

Kwon does not explicitly teach the upper electrode including a noble metal.

However, noble metal such as ruthenium is a known material in semiconductor art for forming capacitor's electrode as shown by Lin ([0041]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ a well known noble metal such as ruthenium as shown by Lin to replace the material in the lower electrode of Kwon, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for a specific application.

14. Claim **12** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon et al. (US Patent No. 5,195,018) in view of Lin et al. (US Patent Application Publication No.

2004/0262663) and further in view of Marsh (US Patent Application Publication No. 2003/0045048).

Regarding claim **12**, the combination of Kwon and Lin discloses the claimed invention of claims 7 and 8 except for forming the titanium oxide layer 4 by atomic layer deposition (ALD).

However, ALD is a known method in semiconductor art for forming (depositing) metal oxide layer of a capacitor as shown by Marsh ([0020]).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the titanium oxide layer by ALD method as shown by Marsh instead of LPCVD method taught by Kwon, in order to significantly enhance the dielectric constant and decrease leakage current ([0024]).

Regarding claim **14**, the combination of Kwon, Lin and Marsh discloses thickness of the titanium oxide layer 4 is less than approximately 50 Å (Kwon, column 3, line 13 – 15)

15. Claim **13** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon et al. (US Patent No. 5,195,018) in view of Lin et al. (US Patent Application Publication No. 2004/0262663), and further in view of Marsh (US Patent Application Publication No. 2003/0045048).

Regarding claim **13**, the combination of Kwon, Lin and Marsh discloses the claimed invention of claims 7, 8, and 12 and shows forming the titanium oxide layer as the instant claim but fails to teach forming the titanium oxide layer in a deposition chamber.

Kwon/Lin/Marsh thus further fail to teach the various steps such as supplying a titanium source, supplying an oxidizer (to supply oxide to form the titanium oxide) as claimed.

However, forming a titanium oxide layer in a deposition chamber is a method by which one of ordinary skill in the art at the time the invention was made would use. See, for example, Won, paragraph [0018] (Won (US Patent Application Publication No. 2002/0115306).

Since forming a titanium oxide layer in a deposition chamber is a method by which one of ordinary skill in the art at the time the invention was made would use to provide titanium oxide, such forming would have been obvious. As for the various specific steps as claimed (namely: supplying a titanium source to an upper portion of the dielectric layer in a chamber; purging an inside of the chamber; supplying an oxidizer; purging the inside of the chamber; and repeating the supplying the titanium source, purging, supplying a oxidizer and the purging at least once), the various specific steps as claimed invariably result in the titanium oxide therefore manipulating such various specific steps would have been obvious.

16. Claim **17** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon et al. (US Patent No. 5,195,018) in view of Lin et al. (US Patent Application Publication No. 2004/0262663) and further in view of Won (US Patent Application Publication No. 2002/0115306).

Regarding claim **17**, the combination of Kwon and Lin discloses the claimed invention of claims 7 and 8 and a thermal treatment process being carried out for the dielectric and the titanium oxide layer (column 3, line 47 – 49).

Kwon and Lin do not explicitly show the temperature for the heat treatment is at a temperature lower than a crystallization temperature of the dielectric layer.

However, Won shows dielectric layer being annealed between about 200^0 C to about 700^0 C ([0023] and [0043]) which is below the crystallization temperature of the dielectric layer at 750^o as stated in the instant application specification page 5, line 34 and page 6 line1.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have the heat treatment step of Kwon performed at a temperature lower than a crystallization temperature of the dielectric layer as shown by Won, in order to relax any residual tress between layer 3 and 4 (Kwon, column 3, line 49 and 50) and to solve the leakage problem (Won, [0008]).

17. Claim **18** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon et al. (US Patent No. 5,195,018) in view of Lin et al. (US Patent Application Publication No. 2004/0262663) and further in view of Won (US Patent No. 6,472,319)

Regarding claim **18**, the combination of Kwon and Lin discloses the claimed invention of claims 7 and 8 and a thermal treatment (curing) process being carried out subsequent to the formation of the upper electrode 5 (column 3, line 47 – 49).

Kwon and Lin do not explicitly show the heat treatment (curing) process being carried out in an oxygen atmosphere at a temperature from about 350^0 C to about 450^0 C.

However, won shows the resultant structure undergoing a thermal treatment under an atmosphere including oxygen at a temperature range 300^0 C to about 500^0 C (column 3, lines 20 – 24).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to have the resultant of Kwon undergoing the heat treatment (curing) in an oxygen atmosphere at a temperature from about 350^0 C to about 450^0 C (which is lower than the oxidation temperature of the upper electrode) as shown by Won, in order to prevent the upper electrode from oxidizing (column 3, lines 24 and 25.)

18. Claim **19** are rejected under 35 U.S.C. 103(a) as being unpatentable over by Kwon et al. (US Patent No. 5,195,018) in view of Marsh (US Patent Application Publication No. 2003/0045048) and Lin et al. (US Patent Application Publication No. 2004/0262663).

Regarding claim **19**, Kwon discloses a method of forming an integrated circuit device (column 1, lines 7 – 16) comprising:

forming a lower electrode 2 (figure 1A, column 2, lines 60 and 61) of a capacitor C on an integrated circuit substrate 1 (figure 1; column 1, lines 14 – 17 and column 2, lines 53 – 56);

depositing a tantalum oxide layer 3 (figure 1B) on the lower electrode 2 (column 2, lines 62 – 67);

depositing a titanium oxide layer 4 (figure 1D; column 2, lines 68, 69 and column 3, lines 5 and 6) on the tantalum oxide layer;

thermally treating the titanium oxide layer and the tantalum oxide layer (column 3, lines 47 – 50);

forming an upper electrode 5 (figure 1F, column 3, lines 40 – 46) on the titanium layer 4; and

curing (thermal treatment process) the upper electrode (column 3, lines 40 – 46).

Kwon fails to show depositing the titanium oxide layer 4 by ALD.

However, ALD is a known method in semiconductor art for forming (depositing) metal oxide layer of a capacitor as shown by Marsh ([0020]).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the titanium oxide layer of Kwon by ALD as shown by Marsh, in order to significantly enhance the dielectric constant and decrease leakage current ([0024]).

In addition, Kwon does not show the upper electrode 5 is made of Ruthenium.

However, noble metal such as ruthenium is a known material in semiconductor art for forming capacitor's electrode as shown by Lin ([0041]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ a well known noble metal such as ruthenium as shown by Lin to replace the material of the lower electrode of Kwon, since it has been held to

be within the general skill of a worker in the art to select a known material on the basis of its suitability for a specific application.

19. Claim **20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon et al. (US Patent No. 5,195,018) in view of Ahn et al. (US Patent Application Publication No. 2004/0175882) and Lin et al. (US Patent Application Publication No. 2004/0262663).

Regarding claim **20**, Kwon discloses a method of forming an integrated circuit device (column 1, lines 7 – 16) comprising:

forming a lower electrode 2 (figure 1A, column 2, lines 60 and 61) of a capacitor C on an integrated circuit substrate 1 (figure 1; column 1, lines 14 – 17 and column 2, lines 53 – 56);

depositing a dielectric (tantalum oxide) layer 3 (figure 1B; column 2, lines 62 – 63) on the lower electrode 2;

depositing a titanium oxide layer 4 (figure 1D; column 2, lines 68 – 69 and column 3, lines 5 – 6) for a barrier layer on the dielectric layer 3;

thermally treating the titanium oxide layer 4 and the dielectric layer 3 (column 3, lines 47 – 50);

forming the upper electrode 5 (figure 1F, column 3, lines 40 – 46) on the titanium oxide layer 4; and

curing the resultant structure (column 3, lines 47 – 58).

Kwon fails to show the dielectric layer is a hafnium oxide layer.

However, Ahn shows for forming a capacitor, a method includes forming a dielectric layer containing hafnium oxide on the first conductive layer by atomic layer deposition ([0096])

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the dielectric layer comprise forming a hafnium oxide layer on the lower electrode as shown by Ahn to replace the tantalum oxide of Kwon, in order to have minimal reactions with a silicon substrate or other structures (abstract).

In addition, Kwon does not show the upper electrode is made of Ruthenium.

However, noble metal such as ruthenium is a known material in semiconductor art for forming capacitor's electrode as shown by Lin ([0041]).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to employ a well known noble metal such as ruthenium as shown by Lin to replace the material of the lower electrode Kwon, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for a specific application.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long K. Tran whose telephone number is 571-272-1797. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LKT

August 6, 2005